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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,884	04/12/2001	Steve M. Danziger	L/M-102-DIV	2718
7590	02/10/2004		EXAMINER	
Ronald R. Snider Snider & Associates P.O. Box 27613 Washington, DC 20038-7613			PERT, EVAN T	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 02/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/832,884	DANZIGER ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Evan Pert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 10 November 2003.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-3 and 5-7 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-3 and 5-7 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 3 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. The solder ball array connections and wire bond connections are necessarily on the same side of the die by the language of claim 1, as best understood.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-3 and 5-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, there are wire bond connections of "the KGD planar surface" which seems to be referring to the antecedent "a planar KGD surface" with the ball array connections. Clarification/amendment is required.

Applicant defines the claimed "end-use device" by process limitations that render the claimed device indefinite because a potential infringer would not be aware of a clear scope of structure being claimed by the process steps [MPEP 2113].

In claim 1, the history of how the device was tested is recited to describe structure. The KGD is "thermal stress tolerance tested prior to mounting," so what one must ask is: what happens to a structure that was "thermal stress tested"? What does it look like compared to when it is not tested?

In claim 2, connections "remain pristine until connected." So what does this mean in the end-use device? Are they then *not* pristine?

In claim 3, aren't the balls and wire bonds necessarily on the same side of the KGD as in claim 1, for thermal stress testing? In claim 1, the balls and wire bonds are claimed as being on the same side, so it is unclear how the scope of claim 3 differs.

In claim 5, connections used for test are "not removed." So what does this mean to the scope of *structure* for a potential infringer? If, in claim 1, the wire bonds are removed, why are they being claimed for *structure* in claim 1? This is a structure claim. A potential infringer must understand scope of *structure* when described by process under judicial precedent [See MPEP 2113].

In claim 6, the *test connections* are "metallurgical connections," but the end-use device was already tested, so the metallurgical connections are no longer connected in the end-use device. So what is the scope of "metallurgical connections" that are *no longer connected*?

For purposes of examination, the claimed end-use device is understood as being a product comprising a properly functional semiconductor chip that has solder ball array connections in electrical connection with wire bond connections on a surface of the chip wherein either the wire bond connections or the solder ball array connections are connected in the end-use and the other is clearly not pristine as a result of thermal stress testing.

***Allowable Subject Matter***

3. Claim 1 would be allowable if rewritten or amended to overcome the rejections under 35 U.S.C. 112, second paragraph, set forth in this Office action.
4. Claims 2, 3, 5, 6 and 7 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.
5. The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not disclose applicant's methodology for thermal stress testing to establish a KGD using an alternative of either solder ball array connections or wire bond connections [see US 6,221,682].

The KGD in an end-use device resulting from the patented '682 method is understood as being a properly functional semiconductor chip that has solder ball array connections in electrical connection with wire bond connections on a surface of the chip wherein either the wire bond connections or the solder ball array connections are electrically connected in the end-use, while the other connections are clearly not pristine as a result of thermal stress testing.

Applicant's end-use device may be considered more reliable because the actual connections to the chip in the end-use device can be pristine when connected in the end-use even though the chip was thermal stress tested using metallurgical connections.

***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703-308-1233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ETP  
February 6, 2004

  
**EVAN PERT**  
**PRIMARY EXAMINER**